2019 IEEE INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY, SIGNAL & POWER INTEGRITY

CALL FOR ABSTRACT REVIEWED PAPERS

The technical program of the **2019 IEEE International Symposium on Electromagnetic Compatibility, Signal and Power Integrity** will include an opportunity for EMC and SI/PI engineers and researchers to write and present Abstract Reviewed Papers. Abstract Reviewed Papers can provide unique opportunities to socialize among EMC and SI/PI engineers and researchers within the renowned IEEE conference environment and to exchange experiences and ideas. This special program will help build a professional community that benefits not only the development of the technologies but also members' professional careers and can lead us to reduce ever-increasing gaps between rapidly changing modern electronic industry and computational analyses and traditional IEEE conferences.

To accommodate the busy schedule of practitioner engineers, and/or new and emerging concepts, only a one-page extended abstract is required for the initial submission for Abstract Reviewed Papers. The submitted abstract will be reviewed by the Technical Paper Committee of the 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal and Power Integrity according to the acceptance criteria indicated below. If accepted a one-page extended abstract will be published in the symposium proceedings and the author will present his or her material in a technical session at the symposium. The author will also be invited to submit a full-length paper (up to 6 pages) for publication in the IEEE Journal on Electromagnetic Compatibility Practice and Applications (J-EMCPA), which contains substantial additional technical material compared to the 1 page abstract published in the symposium proceedings. Together with the invitation the authors get review comments and feedback from the discussion provided by the session chair.

We invite you to be part of this new technical community and look forward to meeting you in New Orleans, Louisiana USA.

GUIDELINES FOR AUTHORS & SUBMITTAL PROCEDURES

- **An extended abstract with approximately 500 words describing paper concept and results.**
- **Choice of presentation format (traditional oral or poster).**

**** During the electronic submission process, a unique author code will be created for tracking purposes.**
After abstract is accepted, further instructions on final paper submission will be provided.

Submissions are reviewed anonymously, so please do not include author names or affiliations on the submitted abstract.
Failure to comply with submission requirements may result in rejection.

PAPER ACCEPTANCE PROCEDURES & CRITERIA

Importance of Topic: Does it directly relate to the EMC/SI/PI community?

Technical Sophistication and Depth: Does it present significant information, contribution, advancement, application or refinement of the state of the art? Does it bring the reader to a higher level of knowledge than is currently available from other sources?

Novelty and Originality: Does it propose a new and unique concept or expand on an existing premise from a unique point of view?

Submissions are reviewed anonymously.

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AUTHOR SUBMISSION SCHEDULE

- **Initial one-page Extended Abstract:** October 1, 2018 to February 16, 2019
- **Acceptance Notification:** March 23, 2019
- **Final one-page Extended Abstract Due:** April 19, 2019

PAPER TOPICS

High-Speed Link/Parallel Bus/Memory Interface Design
- Serial link design and performance analysis
- Parallel bus design and analysis in on-board or system-in-package
- Various memory interface design and analysis
- Advanced on-chip or 2.5D/3D signal interface design and analysis
- Transceiver or driver modeling including IBIS
- Signaling analysis including equalization and coding

Jitter and Noise Modeling, Analysis, and Mitigation
- BER analysis, modeling, and measurement
- Jitter and noise modeling and measurement techniques
- Jitter decomposition techniques
- Jitter and noise sensitivity modeling and analysis
- Crosstalk modeling and mitigation

Aeronautics and Space EMC
- EMC Analysis, Design and Performance

System-In-Package (SiP)
- 3D IC and TSV modeling and analysis
- Timing models and closure in SiP
- Special numerical techniques for 3D integration

Passive Channel Component Modeling and Measurement Techniques
- De-embedding techniques
- High-frequency measurement techniques and models
- Interconnect design and optimization
- Material characterization and modeling
- Frequency and time domain measurement techniques
- Die/package/board SI/PI co-design

Numerical Modeling and Simulation Techniques for Interconnects
- High-frequency and broadband modeling techniques
- Causality and passivity detection and enforcement algorithms
- Measurement and modeling correlation
- Electrical and thermal co-simulation techniques
- Numerical modeling approaches and results for complex environments

Power Integrity Analysis and Power Distribution Network (PDN) Design
- System-level PDN modeling and design
- On-chip and off-chip PDN design and analysis
- On-chip and off-chip regulator modeling and performance analysis
- SI/PI co-optimization and design

EMC Measurements and Interference Control
- Advances in interference control techniques
- Measurement methods and instrumentation
- PCB/connector/cable design for EM emission mitigation
- Standards and Regulations

EMC Modeling and Simulation
- Advances in modeling and simulation methods
- Validation methods
- Applications

ESD, Transients and Immunity
- System-level ESD
- IC/component immunity
- High-power electromagnetics

Wireless EMC
- RF Interference
- Wireless coexistence
- MIMO testing
- Innovative components

EMC, EMI, SI, PI, Standards and Standardization

All other EMC and SI/PI Topics

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